SYSTEM AND METHOD FOR EFFICIENTLY TESTING A LARGE RANDOM ACCESS MEMORY SPACE

ABSTRACT OF THE DISCLOSURE

A system for, and method of, allowing conventional memory test circuitry to test parallel memory arrays and an integrated circuit incorporating the system or the method. In one embodiment, the system includes: (1) bit pattern distribution circuitry that causes a probe bit pattern generated by the memory test circuitry to be written to each of the memory arrays, (2) a pseudo-memory, coupled to the bit pattern distribution circuitry, that receives a portion of the probe bit pattern and (3) combinatorial logic, coupled to the pseudo-memory, that employs the portion and data-out bit patterns read from the memory arrays to generate a response bit pattern that matches the probe bit pattern only if all of the data-out bit patterns match the probe bit pattern.